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Memristive Circuits for On-Chip Memories

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Abstract

In less than a decade, memristors have evolved from an emerging device technology, to a promising circuit concept, and now a commercial product. This accelerated development is due to the importance of memristor devices, which pro- vide greater capacity while reducing power and latency in computer memories. The research described in this dissertation explores circuits composed of memristor devices and design methods to enhance the performance of memristor devices in memory systems.

The dissertation begins with an introduction to memristor device technologies. Physical descriptions of metal-oxide resistive RAM (RRAM) and spin torque transfer magnetoresistive RAM (STT-MRAM) are presented. Classic CMOS memory organization and technology are also reviewed.

Several memory cells, memory array topologies, and memristor based circuits are presented. A novel RRAM based flip flop is described. This circuit, coupled with a highly threaded architecture, demonstrates up to 40% improvement in performance with a modest area overhead of 2.5% as compared to conventional microprocessors. An STT-MRAM based cache is described with a magnetic field assistance mechanism that reduces the switching latency of an individual device by four. This cache reduces energy by 55% as compared to an SRAM subsystem, and a 20% improvement over STT-MRAM based caches discussed in the literature. Additional circuits, design methods, and physical topologies are presented to improve the sense margin, reduce area, and increase bit density of memristor based memories.

Memristor devices are an emerging technology capable of reshaping the computational process. Insight into the design of memristor memories is provided in this dissertation with solutions to improve the performance of memristor based memories.